

A Comparison of MOS PLAs

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There is no universal agreement about the relative merits and long-term advantages of nMOS, CMOS-SOS and CMOS-Bulk technologies. Fundamental limitations on line widths and power loading strongly affect the final geometry size. However, the geometrical design rule spacings and electrical rules may prevent a promising technology from reaching its full potential.

This paper discusses PLA designs in three MOS technologies: nMOS, CMOS/SOS and CMOS-Bulk. The purpose of this paper is not to introduce a new and exciting PLA design, nor is it to recommend one fabrication technology over another. Its purpose is to use PLAs as a standard, hopefully familiar layout strategy so that new designers can get a better understanding of the advantages and disadvantages of all three technologies from a designer's viewpoint. It is hoped that this paper will provide more data to those who must select a technology for their integrated circuit fabrication.

The nMOS PLA

The PLA shown in figure 1 is an nMOS implementation of the traffic light controller from [Mead 1980]. The PLA has three inputs, ten minterms, five outputs and two feedback terms. The inputs and outputs connect at the bottom. The AND-plane is on the left and the OR-plane is on the right. All the PLA examples in this paper are arranged like this.

Both the AND-plane and the OR-plane in the nMOS PLA are composed of NOR gates, so the input drivers invert the input signals and the output drivers invert the results to give an OR of ANDs output.

The CMOS-Bulk PLA

A precharged dynamic CMOS Bulk PLA is shown in figure 2. This PLA is based on a design by C. Seitz [Seitz 1982]. The PLA AND-plane is composed of NAND gates which are precharged high. Between the planes is a precharged inverter, and the outputs are inverted, yielding a NAND-NOT-NOR-NOT sequence, which gives the OR of ANDs.

The PLA programming for the PLA in figure 2 is the same as the programming for the NMOS PLA. Although the array cells are approximately the same size, the drivers for the CMOS design are much larger and the CMOS design has an inverter and precharge circuitry between the planes.

There are four causes of the greater size. First, CMOS Bulk has geometrical design rules which require large spacing at well boundaries [Griswold 1982]. Leaving the P-well requires an 8 lambda metal between pieces of diffusion. When contacts and contact to transistor spacing are added, the minimum distance between pullup and pulldown is 18 lambda, compared to 4 lambda for NMOS. Of course, the CMOS pullup is a minimum length transistor, so about 6 lambda is saved. The result is a 8 lambda difference for each inverter.

The second cause of greater area is the need to route the input to the inverter to both the pullup and the pulldown. The added area needed for the route is not great, but the routing constrains the topology of the resulting layout.

The third cause of greater area is the need in CMOS Bulk to tie the P-wells to

ground and the substrate to VDD (when using a P-well technology). Liberal use of these contacts prevents latchup, the bane of all CMOS Bulk chips.

The fourth cause of greater size is simply greater complexity of the logic caused by the inverter between the planes of the PLA.

The CMOS-SOS PLA

Figure 3 shows a CMOS SOS PLA. This is another dynamic PLA based on a design by C. Seitz. Overall, the PLA is about the same size as the nMOS PLA. This is because CMOS SOS does not suffer from two of the four difficulties of CMOS Bulk.

CMOS SOS does not have the well-crossing restriction of CMOS Bulk, but in order to cross the P-doping boundary in diffusion, one must connect the two kinds of diffusion together with a split contact. The split contact requires only about an eight lambda separation between pullup and pulldown. Again, the pullup is smaller, so the overall size of the inverter is about the same as nMOS.

CMOS SOS does not require the substrate contacts that Bulk does, but it does suffer the topological problems of all CMOS technologies. The result is that the dynamic CMOS SOS PLA is approximately the same size as the static NMOS PLA. The SOS PLA design also has an inverter between the planes of the PLA, but the inverter is smaller in SOS because the split contact takes less area than the metal strap to cross the P-well in Bulk.

Static versus Dynamic PLAs

Dynamic nMOS PLAs can certainly be built, but the only advantage to them is improved speed. In contrast, the area advantages of dynamic PLAs in CMOS are immense. In both SOS and Bulk, precharging removes the need for the pullup structure (or the pulldown structure, depending on the type of precharging). Figure 4 shows a 2 input by 2 minterm part of a dynamic CMOS Bulk PLA next to a similar part for a static PLA. The pullup structure immediately doubles the area, since another path through the inputs is needed. The Bulk also requires a large separation between the two types of substrate, as mentioned above.

One advantage of the nMOS PLA over the CMOS PLAs is that dense static nMOS PLAs can be built. Static circuitry runs slower, but is more reliable, since a single alpha particle cannot change the charge on a precharged node and cause an incorrect result. Thus, designers who want a static CMOS PLA for high reliability may be forced to use a static PLA which is twice the area as the less reliable dynamic PLA.

PLA measures

A PLA can be characterized by the number of inputs, outputs, minterms and feedbacks. The table below defines some measurements for MOS PLAs. The measurements are shown on the schematized PLA drawing in figure 5.

A_x	And plane cell x dimension.
A_y	And plane cell y dimension.
O_x	Or plane cell x dimension.
O_y	Or plane cell y dimension.
S	Separation between planes.
B	Maximum y dimension of input buffer and output buffer.
F	Y dimension wiring space for one feedback wire.
T	Y dimension of logic above the planes.
L	X dimension of logic to the left of the And plane.
R	X dimension of logic to the right of the Or plane.
X	$X \text{ dimension} = L + R + S + (\text{inputs} + \text{feedbacks}) * A_x + (\text{outputs} + \text{feedbacks}) * O_x$
Y	$Y \text{ dimension} = B + T + \text{feedbacks} * F + \text{minterms} * \text{Max}(A_y, O_y)$
A	$\text{Area} = X * Y$

These measurements do not give an exact measure of PLA size for a given number of inputs, outputs, and minterms since most PLAs require some additional power or ground connections for large arrays.

The table below summarizes some area measurements of MOS PLAs. These PLAs are not necessarily optimal, and should be used as order-of-magnitude guesses for comparing the overall performance of each kind of technology. All measurements are in lambda.

	nMOS	CMOS-SOS	CMOS-Bulk
A_x	14	14	16
A_y	7	8	9
O_x	7	11	7
O_y	7	8	9
S	13.5	43	73
B	60.5	37	121
F	5	4	4
T	14	7	23
L	14	7	15
R	7	0	24

The table below compares sizes of PLAs for the traffic light controller given in [Mead 1980]. The traffic light controller has three inputs, five outputs, two feedback terms and ten minterms. The nMOS PLA is static, the CMOS PLAs

are both dynamic.

	nMOS	CMOS-SOS	CMOS-Bulk
X	153.5	197	251
Y	154.5	152	242
A	23716	29944	60742

Conclusion

The advantages of PLAs over other layout strategies is their density and regularity as well as the ability of the designer to automatically lay out the logic. These advantages are even greater in CMOS, which has more difficult wiring constraints because signals must be present in both the pullup and pulldown of a restoring logic gate.

However, PLAs may not be as attractive layout strategy in CMOS due to their large size. Dynamic PLAs are much smaller, and dynamic CMOS SOS PLAs do not differ considerably in area from their NMOS counterparts.

One of the advantages of CMOS technology over NMOS its relatively high reliability and radiation hardness. In order for a particular part to have these properties, though, the designer must avoid dynamic storage nodes. Therefore, dynamic PLA structures would be unacceptable, and the designer must resign himself to using PLAs that are several times the area of the NMOS PLA.

Acknowledgements

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References

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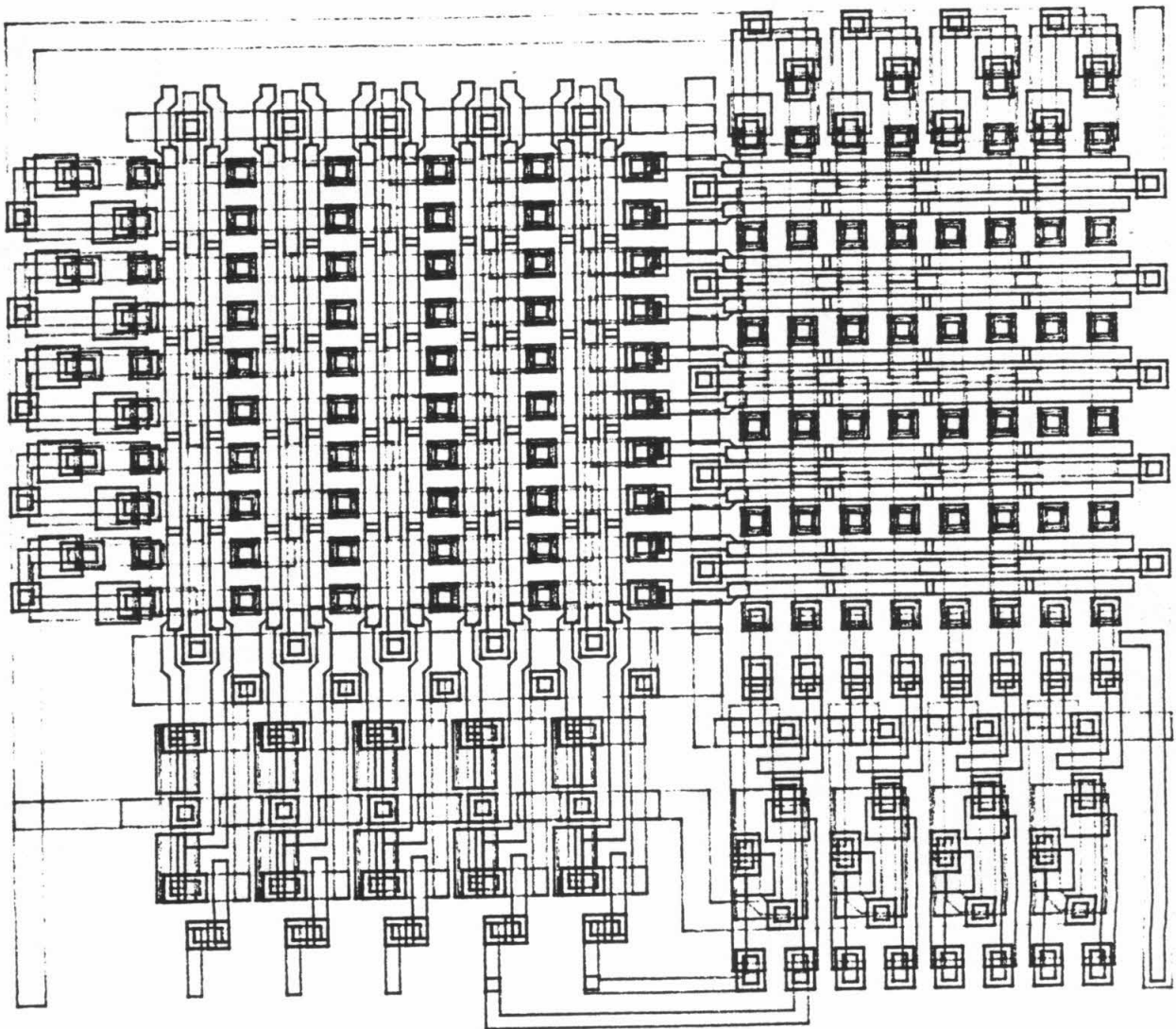


Figure 1. NMOS Traffic Light Controller PLA.

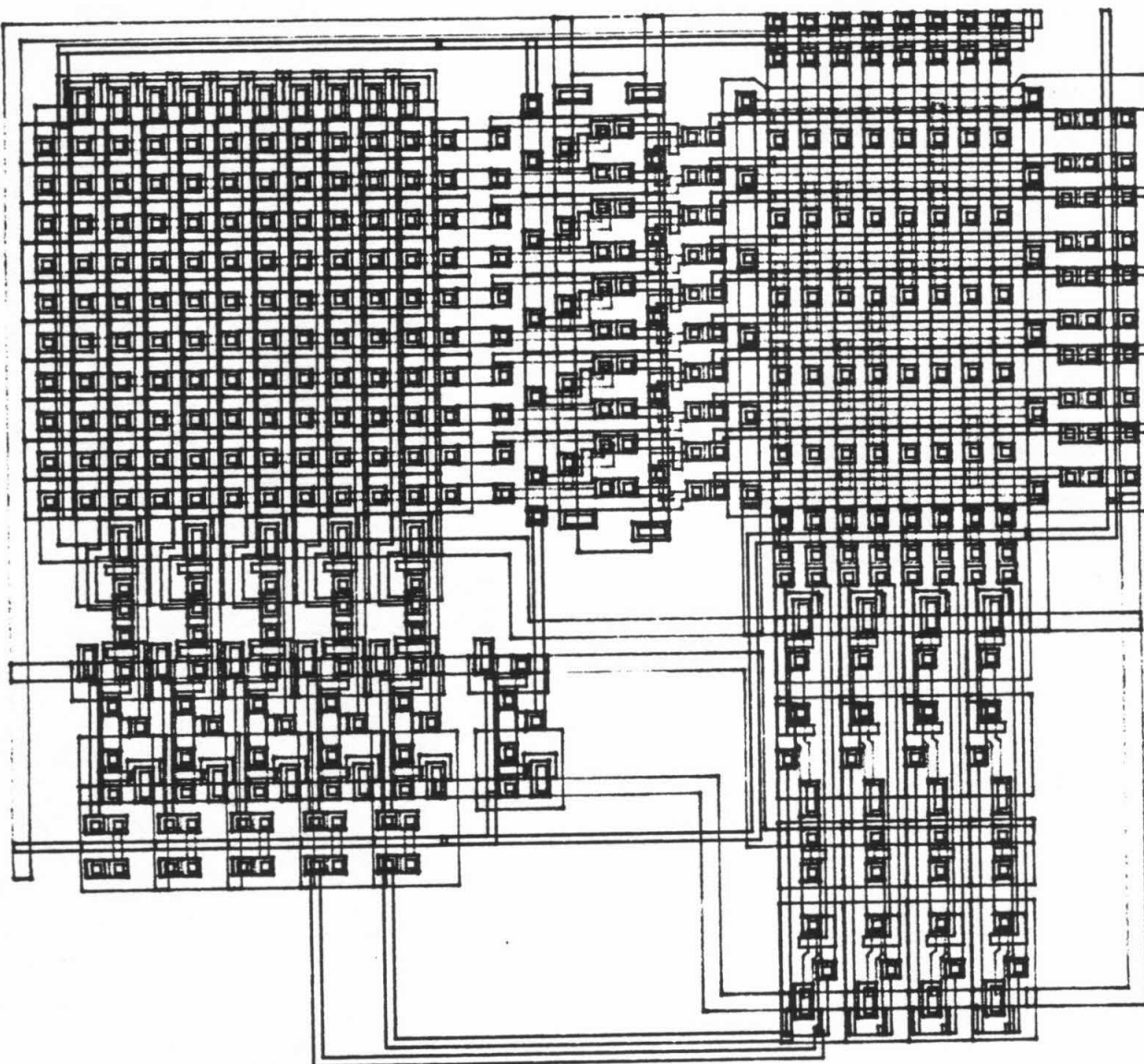


Figure 2. CMOS Bulk Traffic Light Controller PLA.

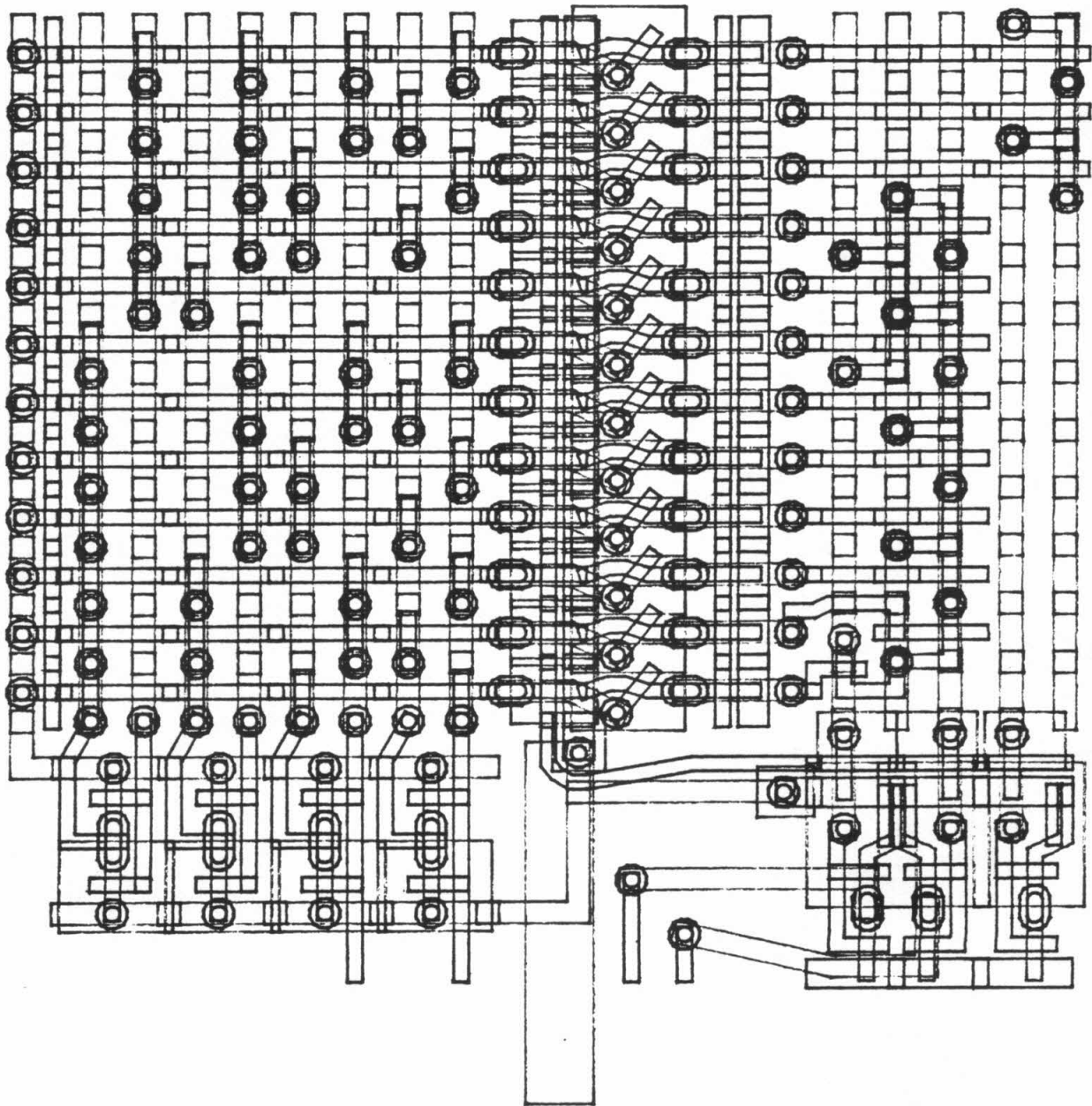


Figure 3. CMOS-SOS PLA.

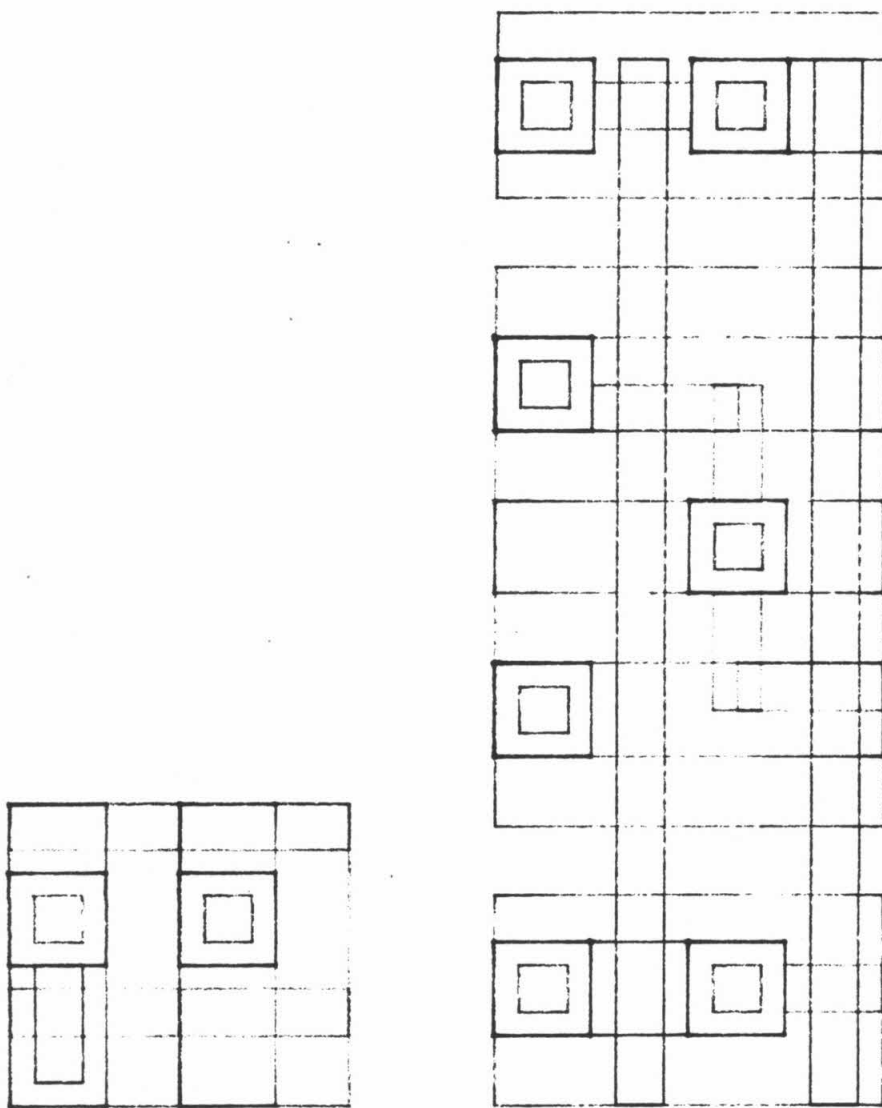


Figure 4. Comparison of Sizes of Dynamic versus Static CMOS Bulk PLA AND-Plane Cells.

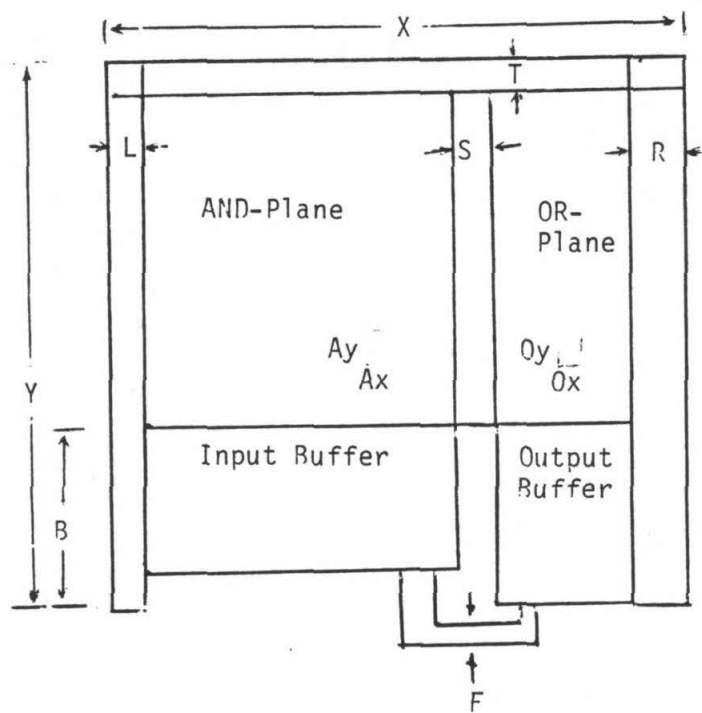


Figure 5. PLA Measurements.